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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/410,928	10/01/1999	ANDREW M. JONES	99-TK-254	7656

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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 11/26/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/410,928	JONES ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed August 14, 2003 in response to PTO Office Action dated May 13, 2003. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-16 have been presented for examination in this application. In response to the last Office Action, claims 1 and 9 have been amended.

Claim Objections

Claims 12 and 16 are objected to because of the following informalities:

Regarding claim 12:

The Examiner believes that "module" in line 2 should be replaced with –unit— in order for the claim limitation to correspond to the "processing unit" of claim 9, line 2.

Regarding claim 16:

The word "casing" in line 7 should be replaced with –causing—in order to correct a misspelling.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12-14 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 12 recites the limitation "the cache state" in line 4. There is insufficient antecedent basis for this limitation in the claim. The limitation "cache state" had not been previously recited.

Claim 13 recites the limitation "the cache" in line 3. There is insufficient antecedent basis for this limitation in the claim. The limitation "the cache" of line 3 had not been previously recited as relating to the cache coherency transaction. The Examiner believes that a limitation such as --corresponding to the cache coherency transaction--, or the like, could be included at the end of claim 13 to better explain the claimed subject matter.

Claim 14 recites the limitation "the system component" in line 9. There is insufficient antecedent basis for this limitation in the claim. The limitation "system component" had not been previously recited.

Regarding claims 14 and 16:

Regarding claims 14 and 16, the preamble for each claim recites "the step of executing further comprises...". Parent claim 9 previously recited the limitation "causing the processing unit to execute a cache coherency operation". It is unclear to

the Examiner whether the limitation "the step of executing", found in claims 14 and 16, is analogous to "wherein the step of causing the processing unit to execute the cache coherency operation is...", a limitation found in claim 11, where claim 11 is also dependent upon parent claim 9.

Claim 16 recites the limitation "the system component" in line 9. There is insufficient antecedent basis for this limitation in the claim. There is insufficient antecedent basis for this limitation in the claim. The limitation "system component" had not been previously recited.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-4 and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. (US# 6,418,514).

Regarding claims 1 and 9, Arimilli et al. teaches a **computer system** including a **memory system** (Fig. 7, cache (56a)). Arimilli et al. teaches including the MESI protocol within the multi-processor computer system (abs., lines 1-2), where the Shared (S) value corresponds indicates that two or more caches each hold a valid copy of a memory block (col. 8, lines 43-55). The MESI protocol makes any block in the cache of Arimilli et al. to be sharable amongst the multi-processors as recited by Arimilli et al., thus each block of the cache **memory** could be seen as an individual **shared memory**. Cache (56a) contains at least one queue, including a cache operations queue (68a). The cache operations queue corresponds to the **transaction-based bus mechanism** as claimed, in that the operations queue contains a serialized list of cache operations that results in a bus transaction (col. 13, lines 29-35). As seen in Figure 7, the cache operations queue is contained within cache memory, which is coupled to **a (single) processor** via processor bus (66a). Figure 7 also illustrates other **system components** coupled to the cache operations queue. The claim limitation "coupled" is not limited to the coupling of system components with a direct connection to the cache operations queue. A **(first) cache coherency request**, issued by a processor or higher-level cache associated with cache (56a) is made in order to claim exclusive ownership of a memory block, where exclusive ownership corresponds to the coherency aspect of the claim limitation. The operation is posted in the operations queue, and then the processor or higher-level cache issues one or more instructions in order to carry out the

cache coherency command that was placed in the operations queue (col. 13, lines 44-54). Another operation regarding multi-processor cache line requesting to another cache is also taught by Arimilli et al. (col. 12, lines 17-24). Thus, **in response to the request**, the cache coherency operation is performed.

Regarding claims 2 and 10, the first request disclosed above is performed without the use of an interrupting mechanism.

Regarding claims 3 and 11, the LRU unit (62a) is issued instructions to carry out for the purpose of selecting the memory block for eviction, which is a part of the cache coherency operation discussed above and taught by Arimilli et al. (col. 13, lines 51-54). Therefore, the LRU init (62a) operates instructions, sent from the processor, **without the assistance of instructions directly executed on the processor**.

Regarding claims 4 and 12, requesting processor (44f) is issued a command, or message, to switch a cache line's MESI value from Invalid to Recent as a **response** to a cache coherency operation (col. 12, lines 19-24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US# 6,418,514) and Spencer (US# 6,295,582).

Regarding claims 5 and 13, the difference between the claimed subject matter and that of Arimilli et al., disclosed supra, is that the claims recites cache flush operation for flushing a cache line, as well as a hit/miss cache item scheme including a writeback operation for cache line hits with modified results. Spencer teaches a cache memory manager enabled to ensure cache space for future operations. The cache memory manager is able to **flush** one or more cache lines of data from the cache according to its own operation (col. 14, lines 2-10).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Arimilli et al. and Spencer before him at the time the invention was made to modify the cache coherency scheme of Arimilli et al. to include the flushing and write-back schemes of Spencer, because then system-wide data coherency could be maintained as well as implementing a function for consistent cache availability for future cache operations, as taught by Spencer.

Regarding claims 6 and 14, Spencer teaches a cache **miss** resulting from a **lookup** in the loading of data from a main memory into the cache (response). On a cache **hit**, the data is already in the cache in an unmodified format and able to be immediately used (col. 4, lines 45-55). On a cache write-hit to a modified line, a dirty bit is set and the cache controller is responsible for writing-back the updated data to the main memory before replacing the data related to the write-hit (col. 5, lines 13-30).

Claims 7, 8, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US# 6,418,514) and Jacobs (US# 6,047,358).

The difference between the claimed subject matter and that of Arimilli et al., disclosed supra, is that claims 7 and 15 recite a cache purge operation for purging a cache line. As part of the copy-back operation, the cache line is marked as invalid (col. 18, lines 58-61) for eviction (**purging**) of the cache line.

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Arimilli et al. and Jacobs before him at the time the invention was made to modify the cache coherency scheme of Arimilli et al. to include the purging and write-back schemes of Jacob, because then system-wide data coherency could be maintained as well as a replacement policy that includes the principles of locality to reduce cache misses, as taught by Spencer.

Regarding claims 8 and 16, as well as a hit/miss cache item scheme including a writeback and invalidation system for cache line hits with modified results. Jacobs teaches that upon a cache miss resulting from a cache **lookup**, the requested item is loaded into the cache (col. 10, lines 58-62). Jacobs also teaches a write access (hit) that results in the cache line incorporating a modified value setting within a copy-back (write-back) coherency policy (col. 10, lines 34-46). As part of the copy-back operation, the cache line is marked as invalid (col. 18, lines 58-61).

Response to Arguments

Applicant's arguments filed August 14, 2003 have been fully considered but they are not persuasive.

Applicant's arguments are directed toward a single processor within the computer system, as claimed. As seen in Figure 7, the cache (56a) is connected to a single processor via bus (66a). Thus, a box could be drawn around at least this single processor, cache, the memory device (52), and possibly any other components and still teach the claimed invention.

Applicant's arguments are also directed toward the inclusion of a cache operations queue. Applicant's arguments recite that the queues of Arimilli et al. are not necessary, and that they do not display two separate properties, although the claim limitations do not recite or preclude such limitations. The cache operations queue of Arimilli et al. teaches the elements of the claim limitations of the transaction-based bus mechanism, as recited above, and thus fulfills the requirements for rejection of the claim limitations.

The Examiner has included additional language within each of the rejection in order to better describe the prior art without producing new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187

DS/BRP

for Donald Sparks
Supervisory Patent Examiner
Art Unit 2187

November 18, 2003